CLAIMS

What is claimed is:

1. A method of updating programmable device configuration code stored in EEPROMs of a system, the system having separate management and system processors, comprising executing a sequence for updating programmable device configuration code on a management processor of the system, the sequence for updating programmable device configuration code further comprising the steps of:

erasing the EEPROMs;

writing at least one block of configuration code to the EEPROMs;

checking for errors after writing the at least one block, the errors including failure of a FIFO to empty, and retrying the step of writing at least one block upon error.

2. The method of Claim 1, further comprising the step of verifying that a file contains configuration code compatible with the system.

3. The method of Claim 2, wherein the step of verifying that a file contains configuration code compatible with the system comprises polling a JTAG bus of the system to determine the configuration of the JTAG bus, and comparing the configuration with a configuration stored in the file.

4. A method of updating programmable device configuration code stored in EEPROMs of a system comprising the steps of:

providing at least one serial bus interconnecting EEPROMs of the system with a common configuration logic;

obtaining a file of configuration code;

verifying compatibility of the file with the serial bus;

erasing at least one EEPROM of the EEPROMs;

writing at least one block of configuration code to the EEPROMs; and

checking for errors after writing blocks, the errors including failure of a FIFO to empty, and retrying the step of writing at least one block upon an error.

5. The method of Claim 4, further comprising the step of soft-booting at least one programmable logic device to load configuration code from an EEPROM of the at least one EEPROMs into the programmable logic device.

6. The method of Claim 5, wherein the system has more than one processor, and further comprising the step of allocating the common configuration logic to prevent simultaneous access by more than one processor of the system.

7. The method of Claim 5, wherein the at least one serial bus interconnecting EEPROMs of the system with a common configuration logic is a plurality of serial busses, and further comprising the step of selecting a particular serial bus of the plurality of serial busses.

8. The method of Claim 5, wherein at least one programmable logic device is an FPGA, and wherein method is executed automatically upon an error loading configuration code from EEPROM into the FPGA.